

【特許請求の範囲】

【請求項1】 直接拡散符号分割多元接続方式を用いた移动通信システムの受信機のCDMAチップ同期回路において、

受信信号に含まれる複数のマルチパス成分の受信タイミングを測定するサーチ手段と、

該サーチ手段で測定した前記受信タイミングに対して、該受信タイミングを中心として、その前後の1チップ周期より短い時間間隔の複数のタイミングで受信を行う複数の受信手段と、

該複数の受信手段の出力を一時記憶するメモリと、

前記複数の受信手段で受信した複数の受信信号のうち、受信品質の最も良い受信信号を一定時間間隔で選択する選択手段と、

により構成されることを特徴とするCDMAチップ同期回路。

【請求項2】 前記選択手段は、伝播路のフェージング周期と比べて短く、且つ、受信品質の平均化処理が可能な時間間隔で、選択する受信信号を切り替えることを特徴とする請求項1に記載のCDMAチップ同期回路。

【請求項3】 前記選択手段は、最も受信品質の良い受信信号の受信タイミングと2番目に受信品質の良い受信信号の受信タイミングの時間間隔があらかじめ定められた時間より短いとき、該2つの受信信号を選択することを特徴とする請求項1に記載のCDMAチップ同期回路。

【請求項4】 前記選択手段は、受信品質の判断を受信信号の電力の大きさにより行うことを特徴とする請求項1に記載のCDMAチップ同期回路。

【請求項5】 前記選択手段は、受信品質の判断を受信信号電力と干渉電力の比により行うことを特徴とする請求項1に記載のCDMAチップ同期回路。

【請求項6】 直接拡散符号分割多元接続方式を用いた移动通信システムのCDMA受信機のCDMAチップ同期回路において、

受信した無線周波数信号をデジタルベースバンド信号に変換する無線受信部と、

前記デジタルベースバンド信号に含まれる複数のマルチパス成分の各々の復調処理を行う複数のマルチパス復調部と、

該マルチパス復調部で復調された複数のマルチパス成分を最大比合成し、受信データを出力するRAKE合成部と、

前記デジタルベースバンド信号のスペクトラムを逆拡散するための逆拡散符号を発生する逆拡散符号発生部と、前記デジタルベースバンド信号に含まれる複数のマルチパス成分の受信タイミングを測定するサーチ手段と、を備え、

前記マルチパス復調部が、

前記逆拡散符号を前記サーチ手段の検出した受信タイミ

ングと一致するように遅延させる遅延手段と、

前記遅延された逆拡散符号を1チップ周期より短い一定の遅延間隔で遅らせた複数の出力端子を持つシフトレジスタと、

前記デジタルベースバンド信号と前記シフトレジスタの出力の各々の相関値を求めることにより前記デジタルベースバンド信号の逆拡散を行う複数の相関器と、

前記複数の相関器の出力を一時的に蓄積するメモリと、前記メモリを一定時間間隔で読み出し、最も受信品質の良い相関器出力を選択する最適値検出手段および選択手段と、

該選択手段により選択された相関器出力を用いて同期検波を行う同期検波手段と、を有することを特徴とするCDMAチップ同期回路。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明はCDMAチップ同期回路に関し、詳しくは移动通信システム、特に直接拡散符号分割多元接続(DS-CDMA)方式を用いた自動車電話・携帯電話システム(セルラシステム)の受信装置、特に基地局受信装置における受信タイミング検出回路に関する。

【0002】

【従来の技術】従来例として、特開平4-347944号公報や、特開平6-284111号公報の「スペクトラム拡散通信装置の同期装置」や、特公平2-39139号公報の「スペクトラム拡散通信方式の受信装置」や、1994年5月に発行されたTelecommunication Industry Association (TIA)による「TIA/EIA INTERIM STANDARD (TIA/EIA/IS-95-A) Mobile Station-Base Station Compatibility Standard for Dual-Mode Wideband Spread Spectrum Cellular System PN-3421 (to be published as IS-95-A) の第6章、第7章」や、1995年4月に発行されたAndrew J. Viterbi著の「Principle of Spread Spectrum Communication」の第3章39ページ～66ページおよび図3.1、図3.2、図3.6」等が挙げられる。

【0003】従来の移动通信システムのうち、符号分割多元接続(CDMA)方式を用いたデジタル自動車電話・携帯電話システム(セルラシステム)として、北米標準方式(TIA-IS95)が知られている。TIAの発行する標準仕様書TIA-EIA/IS-95-Aの第6章には移動局に要求される動作が記述されており、第7章には基地局に要求される動作が記述されている。しかしながら、上記標準仕様書は主に無線インターフェースを規格化するものであるため、変調方式、信号フォーマット等は記述されているが、具体的な受信方法については書かれていない。

【0004】IS-95-Aの下り回線(基地局→移動局)では、情報で変調された複数ユーザのトラフィック

チャネル(TCH)に加えて、情報で変調されていない共通パイロットチャネル(PLCH)が比較的強い電力で送信されており、移動局はこのパイロットチャネルを使って最適な受信タイミングを決めれば良いため、低い E_b/N_0 (E_b は情報1ビット当たりの受信信号のエネルギー、 N_0 は1Hz当たりの雑音と干渉信号の電力密度)のもとで受信タイミングを決定しなければならないという問題は小さかった。しかしながら、パイロットチャネルを強い電力で送信するということは、それだけ、実際に情報を送信するトラフィックチャネルの数を減らさなければならないため、1基地局当たりのユーザ数が減少するという別の問題がある。

【0005】IS-95-Aの上り回線(移動局-基地局)では、共通パイロットチャネルは存在せず、64-ary直交符号で変調と4倍直接拡散を組み合わせた変調方式が採用されている。64-ary直交符号を用いることにより、BPSK、QPSK等と比べて、1シンボル当たりの電力が大きくなること、非同期検波を採用しても同期検波に対する劣化が小さいこと、等のメリットがあるが、受信方式は複雑である。

【0006】IS-95-Aの主要諸元は、チップレート1.2288Mcps、ビットレート9.6kbps、直接拡散の拡散率128倍、である。チップレートが比較的低速であり(狭帯域CDMA)、伝播遅延の瞬時変動幅に比べ、チップ周期が比較的長いので、受信タイミング検出回路の特性が甘くても受信特性の劣化が少なかった。しかしながら、音声に限らず高速のデータ通信を行うためにはビットレート、チップレートを5~10倍程度速くする必要があり(広帯域CDMA)、IS-95-Aでは見えなかった問題点がでてきている。たとえば、チップレート10Mcpsの場合、伝播経路が30m異なるだけで、1チップだけ受信タイミングがずれ、元のタイミングでは受信できなくなる。また、数チップの遅延時間の範囲に複数のマルチパスが重なり合って現れ、ピーク位置がはっきりしないという問題がある。

【0007】従来の受信タイミング検出方式(チップ同期)は、たとえば、参考文献(アンドリュウ J ビタビ、Andrew J. Viterbi 著、Principle of Spread Spectrum Communication)に記載されている。疑似ランダム符号である拡散符号で拡散された信号のタイミングの捕捉は2段階で行われる。すなわち、初期同期捕捉(サーチ)と同期追尾(トラッキング)の2段階に分けられる。

【0008】初期同期捕捉(サーチ)方法は、参考文献の3章4節に説明されているように、相関電力がある閾値を越えるまで、受信タイミングを1/2チップ間隔でずらせながら、シリアルにサーチする方式である。

【0009】同期追尾(トラッキング)はアーリー・レイト・ゲート(early-late gate)あるいはディレイ・ロ

ック・ループ(DLL)と呼ばれる方法で、受信すべき遅延時間の Δt だけ速いタイミングでの相関電力と Δt だけ遅いタイミングでの相関電力を求め、両者の差が0となるように、タイミングを微調整するという方式である。

【0010】上記、初期同期捕捉および同期追尾の方法を多少改善し、回路の共通化とマルチパス伝播路に対するトラッキング機能を追加した方法が、特開平4-347944号公報に記載されている。しかしながら、基本的な動作はビタビの参考文献の方法と同一であり、また、広帯域CDMAにおける課題を解決するものではない。

【0011】また、特公平2-39139号公報には、スライディング相関器を、初期同期捕捉時のみではなく、常時動作させ、新たなパスをサーチする方法が記載されている。同様な記載が特開平6-284111号公報にも見られる。常時新たなパスをサーチすることにより、瞬断時間を短縮することは可能になるが、複数のパスが重なって受信されるとき、短時間に正確なピーク位置を検出することが可能になるわけではない。

【0012】

【発明が解決しようとする課題】CDMA方式を用いた移動通信システムでは、複数の建物、山等で反射され、伝播時間が微妙に異なる複数の伝播経路を経由して受信される、いわゆるマルチパス信号の各々にタイミングをあわせて受信しなければならない。また、周波数の有効利用のため、各チャネルは非常に低い E_b/N_0 環境下で受信できなければならない。

【0013】特に、チップレートが10Mcps程度以上の広帯域CDMA方式の場合、伝播距離が30m変わっただけで受信タイミングが1チップずれてしまい、受信できなくなる。30m程度の伝播遅延差は、基地局と移動局の距離が変わらなくても、伝播経路が多少変動するだけで容易に発生するため、複数のマルチパスが数チップの範囲で重なって受信されると同時に受信パスの変動(新たなパスの出現、消失)が非常に頻繁になるという現象が現れる。

【0014】従来、受信タイミングの同期追尾(トラッキング)に用いられていた遅延ロックループ(DLL)は、マルチパスの各々が分離したピークをもち、且つ、伝播遅延時間が緩やかに連続的に変動する場合に有効な技術であったが、マルチパスが重なって受信され且つ不連続的に遅延時間が変化する広帯域CDMAでは、トラッキング不可能になる場合があるという問題があった。

【0015】本発明の目的は、広帯域CDMA方式を採用した移動通信システムにおいて、低い E_b/N_0 環境で、マルチパス受信タイミング、特に同期追尾(トラッキング)を確実に行うことのできる手段を提供することである。

【0016】この結果、広帯域CDMA受信機の受信品

質を向上し、高速データ伝送を可能とすることを目的とする。

【0017】

【課題を解決するための手段】本発明のCDMA受信機のチップ同期回路は、受信した無線周波数信号をデジタルベースバンド信号に変換する無線受信部（図1の101）と、デジタルベースバンド信号に含まれる複数のマルチパス成分の各々の復調処理を行う複数のマルチパス復調部（図1の112）と、マルチパス復調部で復調された複数のマルチパス成分を最大比合成し受信データを出力するRAKE合成部（図1の107）と、スペクトラムを逆拡散する符号を発生する逆拡散符号発生部（図1の108）と、複数のマルチパス成分の受信タイミングを測定するサーチ手段（図1の111）と、より構成され、特にマルチパス復調部は、逆拡散符号をサーチ手段の検出した受信タイミングと一致するように遅延させる遅延手段（図1の109）と、遅延された逆拡散符号を一定の遅延間隔たとえば $1/4$ チップ間隔で遅らせた複数の出力端子を持つシフトレジスタ（図1の110）と、デジタルベースバンド信号とシフトレジスタの各出力との相関値を求めることにより受信信号の逆拡散を行う複数の相関器（図1の102）と、複数の相関器の出力を一時的に蓄積するメモリ（図1の103）と、メモリから一定時間間隔で読み出し、最も受信品質の良い相関器出力を選択する最適値検出手段および選択手段（図1の104、105）と、選択された相関器出力を用いて同期検波を行う同期検波手段（図1の106）と、により構成されている。

【0018】図1に示すように、サーチ手段で検出した受信タイミングを基準として、たとえば $1/4$ チップ間隔でずらせたタイミングで同時に相関計算（逆拡散）を行い、逆拡散後の受信品質の最も良いタイミングの信号を後で選択することにより、受信タイミングが不連続的に変化する場合でも確実な受信が可能になる。また、DLLと異なって、複数のパスが完全に分離されずに重なって受信されるような伝播環境でも確実に受信レベルがピークとなるタイミングを捕捉することが可能になる。

【0019】また、サーチ手段は、たとえば $1/4$ チップ精度で正確な受信レベルがピークとなるタイミングを検出する必要がなく、各マルチパス復調部の捕捉できる範囲におさまる精度でピークのタイミングを検出できれば良い。したがって、サーチ手段の検出精度を押えるかわりに検出速度を早めることが可能になる。

【0020】

【発明の実施の形態】次に本発明の一実施の形態について図面を参照して説明する。

【0021】図2は、本発明を適用する、広帯域CDMAにおける遅延時間と受信レベルの関係をモデル化して示すグラフである。

【0022】この図は、2つの独立したマルチパス群を

もち、1つのマルチパス群は $1/2$ チップずつ離れた3つのパスが互いに重なりあって受信される場合をモデル化している。

【0023】図2のうち上のグラフでは、第1のパス群の3つのパスは同位相で受信されているため、強め合って中央に大きなピークができています。第2のパス群の3つのパスは、中央のパスが逆位相で受信されているため、打ち消しあって中央の受信レベルは非常に小さくなり、2つのサブピークに分かれて見えている。

【0024】図2のうち下のグラフでは、第1のパス群の3つのパスのうち、最後の1パスが逆位相で受信されているため、ピークの位置がセンターより $1/2$ チップ前にずれて見えている。また、センターより $1/2$ チップ後に小さなサブピークができています。第2のパス群は、最初の1パス以外が逆位相となっているため、ピーク位置がセンターより $1/2$ チップ遅れた位置になっている。

【0025】このように、複数のマルチパスがわずかにずれて重なり合って受信される場合には、各パスの受信タイミングも受信レベルも変化しなくても、互いの位相関係が変化するだけで、受信レベルのピークが揺らぐことが分かる。

【0026】本発明の受信機は、サーチ手段でパス群の位置を検出し、サーチ手段の検出したパス群の各々に対して、マルチパス復調部を割り当て、各マルチパス復調部は、サーチ手段の検出したタイミングをセンターとして、その両側（遅延の少ないタイミングと大きいタイミング、たとえば $\pm 1/2$ チップ、 $\pm 1/4$ チップ）で受信信号を逆拡散する複数の相関器をもち、一定の時間間隔で受信品質の最も良いタイミングの相関器出力（逆拡散信号）を選んで復調することを行うものである。

【0027】図2のうち上のグラフの第2のパス群のように、同じレベルの2つのピークが1チップ以上離れて（すなわち2つのピークに含まれる雑音が独立とみなせる場合）現れる場合、あるいは図2のうち下のグラフの第1のパス群のように1チップ以上離れた位置に比較的大きなサブピークが現れる場合は、2つのピークに対応する相関器出力を取り出し、合成することも可能である。

【0028】図3は、本発明の第1実施例における、信号フォーマットを示す図であり、図3において、PLはパイロットシンボルを示している。

【0029】図3に示すように、フェージング周期と比べて短い一定周期（たとえば0.625ms周期）で既知のパイロット信号が挿入されて伝送され、このパイロット信号を参照信号として同期検波を行う方式の場合、このパイロット周期を区切りとして、複数の相関器出力をメモリに蓄積し、このパイロット周期に含まれる信号の受信品質を各相関器ごとに測定し、最も受信品質の高い相関器出力、および、受信品質の最も高い相関器のタイ

ミング（ピーク位置）から雑音が独立と考えられるだけ離れた位置にサブピークが検出される場合は、このサブピークに対応する相関器出力をメモリより取り出し、パイロット信号をキャリア位相を示す参照信号として同期検波を行う。

【0030】なお、各相関器出力の受信品質の判定方法としては、次のような方法が適用できる。

- ・パイロット信号の受信レベルによる判定。
- ・パイロット信号が複数のシンボルで構成されるとき、その平均値の2乗（信号電力の推定値）と分散（雑音電力の推定値）の比による判定。
- ・パイロット信号部分だけでなく、データ信号部分も使って受信レベルを測定して判定する。
- ・データ部分を仮判定し、仮判定結果で受信データを逆変調することで全データの位相をキャリア位相にそろえた後、その平均値の2乗（信号電力の推定値）と分散（雑音電力の推定値）の比による判定。

【0031】

【実施例】次に本発明の一実施例について図面を参照して説明する。

【0032】図1は、本発明の実施例を示すブロック図である。

【0033】図1を参照すると、本発明のCDMAチップ同期回路は、受信した無線周波数信号をデジタルベースバンド信号に変換する無線受信部101と、デジタルベースバンド信号に含まれる複数のマルチパス成分の各々の復調処理を行う複数のマルチパス復調部112と、マルチパス復調部112で復調された複数のマルチパス成分を最大比合成し受信データを出力するRAKE合成部107と、スペクトラムを逆拡散する符号を発生する逆拡散符号発生部108と、複数のマルチパス成分の受信タイミングを測定するサーチ手段111と、より構成され、特にマルチパス復調部112は、逆拡散符号をサーチ手段111の検出した受信タイミングと一致するように遅延させる遅延手段109と、遅延された逆拡散符号を一定の遅延間隔、たとえば1/4チップ間隔で遅らせた複数の出力端子を持つシフトレジスタ110と、デジタルベースバンド信号とシフトレジスタ110の各出力との相関値を求めることにより受信信号の逆拡散を行う複数の相関器102と、複数の相関器の出力を一時的に蓄積するメモリ103と、メモリを一定時間間隔で読み出し、最も受信品質の良い相関器出力を選択する最適値検出手段104および選択手段105と、選択された相関器出力を用いて同期検波を行う同期検波手段106と、により構成されている。

【0034】マルチパス復調部112は、実伝播環境において、有効なマルチパス数の最大値とハードウェア規模のトレードオフ関係で決定されるが、通常の都市部では1無線信号受信部（1アンテナに対応）当たり4個程度あれば良い。1つのマルチパス復調部112は、サー

チ手段111の示すタイミングをセンターとして、0、 $\pm 1/4$ チップ、 $\pm 1/2$ チップの合計5つのタイミングで相関値を求める5個の相関器102を含んでいる。

【0035】メモリ103は、5個の相関器出力を、パイロットシンボルで区切られた1スロット区間分記憶できれば良い。

【0036】移動機は基地局から移動機に送信されている下り信号にフレーム同期をとって上り信号を送信するため、基地局のサーチ手段111は、1つの基地局のカバーするサービスエリア半径にしたがって、あらかじめ定められ伝播遅延の範囲で、パスサーチを行えば良い。このような基地局用パスサーチ方法は、たとえば特願平8-185103号に記載されているので、あえて説明しない。

【0037】最適値検出手段104の処理方法は上記実施の形態で説明した通りである。

【0038】

【発明の効果】第1の効果は、一定周期（たとえばパイロット信号が挿入される周期）ごとに最適な受信タイミングを微調整できることである。このため、広帯域CDMAにおいて、複数のマルチパスが重なり合って受信されるような伝播環境においても、受信レベルのピークの変動に同期追尾（トラッキング）でき、安定した受信が可能になるという効果がある。

【0039】第2の効果は、サーチ手段の検出精度をゆるめることが可能になることである。このため、サーチを行う際の平均化時間を少なくすることが可能になり、伝播経路が急に变化しても新たなパスを速やかに検出することが可能になるという効果がある。

【図面の簡単な説明】

【図1】本発明の一実施例の構成を示すブロック図である。

【図2】本発明を適用する広帯域CDMAにおける伝播特性（遅延プロファイル）をモデル化してあらわしたグラフであり、伝播遅延時間、受信レベルが変動しないで、パス間の位相関係が変化したときの合成プロファイルの差を比較したグラフである。

【図3】本発明の一実施の形態における信号フォーマットを示す図である。

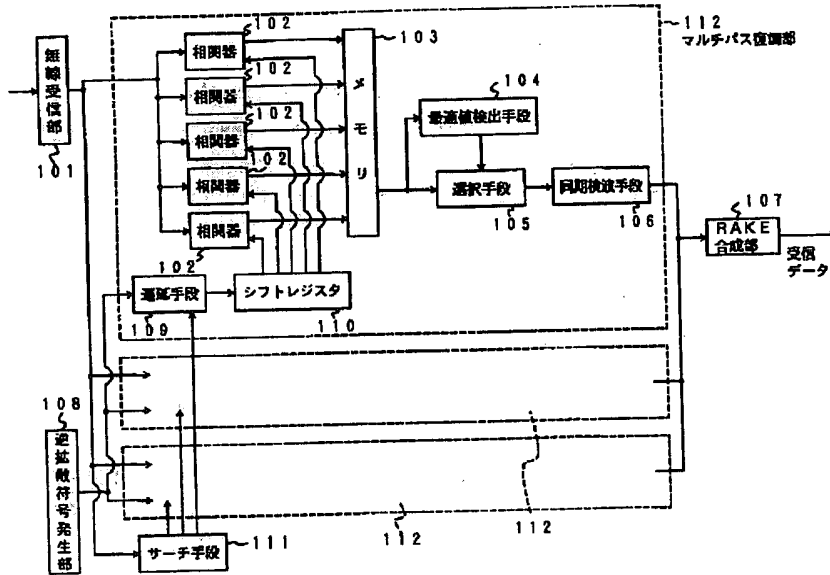
【符号の説明】

- 101 無線信号受信部
- 102 相関器
- 103 メモリ
- 104 最適値検出手段
- 105 選択手段
- 106 同期検波手段
- 107 RAKE合成部
- 108 逆拡散符号発生部
- 109 遅延手段
- 110 シフトレジスタ

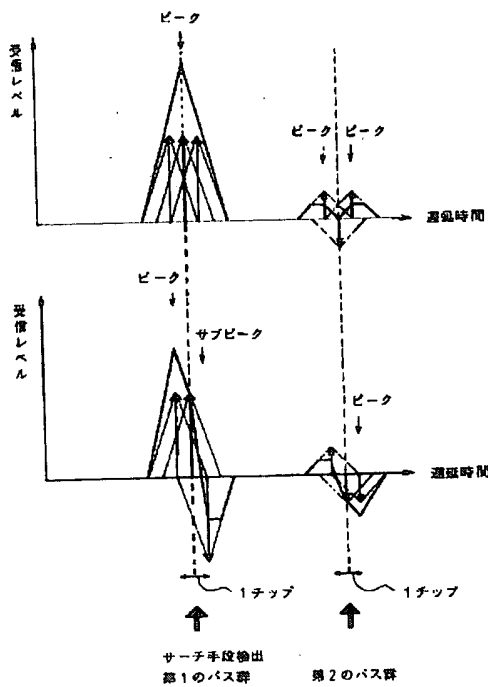
111 サーチ手段

112 マルチパス復調部

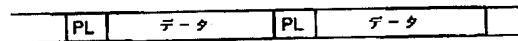
【図1】



【図2】



【図3】



(19)



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(54) CDMA chip synchronization circuit

(57) A CDMA chip synchronization circuit is provided for a mobile communications system employing a wide band CDMA method, especially direct spread code division multiple access (DS-SS) method, and is designed to have a capability to certainly perform detection of multipath receiving timing, particularly synchronous tracking, under a low E_b/N_0 environment where multipaths are received in an overlap manner. Herein, a radio receiver (101) converts radio frequency signals to digital base band signals, whilst a search section (111) detects receiving timing with respect to multipath components contained in the digital base band signals. The detected receiving timing is used as a center position for receiving on a time axis. The radio receiver is connected with multipath receivers (112), each of which contains a number of correlators (102)

which produce correlation values between the multipath components and dc-spreading codes which are delayed by different delay times respectively. Herein, the correlators correspond to prescribed intervals of time which deviate from the center position for receiving on the time axis. Correlator outputs are temporarily stored in a memory (103). Then, the multipath receiver selects a correlator output having a best receiving quality from among the correlator outputs by every prescribed interval of time corresponding to a pilot period, so synchronous detection is performed using the selected correlator output. Outputs of the multipath receivers are combined at a maximum ratio, so that receiving data are produced.

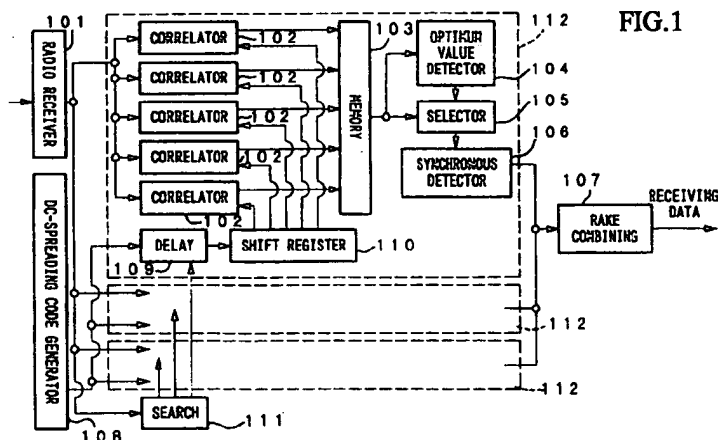


FIG. 1

EP 0 848 503 A2

Description

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to CDMA chip synchronization circuits which are provided in CDMA receivers to perform synchronous detection with respect to receiving timing of radio frequency signals. This application is based on patent application No. Hei 8-333393 filed in Japan, the content of which is incorporated herein by reference.

Prior Art

The CDMA chip synchronization circuit (where 'CDMA' stands for 'Code Division Multiple Access') is provided in the receiver of the mobile communications system, particularly in the receiver of the automobile phone and portable phone system (which will be simply called "cellular system") using the DS-CDMA method (where 'DS-CDMA' stands for 'Direct Spread CDMA'). In other words, the CDMA chip synchronization circuit is used to detect the receiving timing at the base station receiver.

Examples of the spread spectrum communications are disclosed by the papers of Japanese Patent Laid-Open Publication Nos. 4-347944 and 6-284111 both of which relate to the synchronization device for the spread spectrum communications equipment as well as the paper of Japanese Patent Publication No. 2-39139 which relates to the receiver of the spread spectrum communications method, for example. In addition, we can list other information regarding the disclosure of the spread spectrum communications, for example, Chapter 6 and Chapter 7 of the paper entitled "TIA/EIA INTERIM STANDARD (TIA/EIA/IS-95-A) Mobile Station-Base Station Compatibility Standard for Dual-Mode Wideband Spread Spectrum Cellular System PN-3421 (to be published as IS-95-A)" which is published by the Telecommunication Industry Association (TIA) on May of 1994 as well as FIG. 3.1, FIG. 3.2, FIG. 3.6 and pages 39-66 of Chapter 3 of the paper entitled "Principle of Spread Spectrum Communication" which is written by Dr. Andrew J. Viterbi and published on April of 1995.

Among the conventional mobile communications systems, the so-called North American standard method (i.e., TIA IS95) is known as the digital cellular system using the CDMA method. In the standard specification of TIA/EIA/IS-95-A, Chapter 6 describes operations required for the mobile station, while Chapter 7 describes operations required for the base station. However, the above standard specification merely provides standardization for the radio interface. For this reason, the standard specification describes the modulation method and signal formats but fails to describe

the concrete receiving method.

The forward link of IS-95-A (which is used to perform transmission from the base station to the mobile station) performs transmission of pilot channels (PLCH) in addition to transmission of traffic channels (TCH). Herein, the traffic channels are provided for multiple users subjected to modulation by information, whilst the pilot channels are not subjected to modulation by information. Further, the transmission of the pilot channels is performed using relatively intense electric power. Using the pilot channels, the mobile station is capable of determining the optimum receiving timing. So, the mobile station does not so much suffer from a problem that the receiving timing should be determined under low Eb/No (where 'Eb' denotes energy of receiving signals per 1 bit of information; and 'No' denotes electric power density of noise and interference signal per 1 Hz). However, transmission of the pilot channels using the intense electric power results in reduction of a number of traffic channels which are used for actual transmission of information. This causes another problem that a number of users per one base station should be reduced.

On the other hand, no common pilot channels exist in the reverse link of IS-95-A (which is used to perform transmission from the mobile station to the base station). So, the reverse link employs the modulation method corresponding to the 64-ary orthogonal code modulation combined with the quadruple direct spread. Using the 64-ary orthogonal codes, as compared with the BPSK and QPSK (where 'BPSK' stands for 'Binary Phase-Shift Keying' and 'QPSK' stands for 'Quaternary PSK'), it is possible to provide a variety of merits as follows:

It is possible to increase electric power per one symbol. It is possible to reduce deterioration for synchronous detection even if asynchronous detection is employed.

However, the above has complicity in receiving method.

Main elements of the IS-95-A are determined such that the chip rate is set at 1.2288 Mcps, bit rate is at 9.6 kbps and spread rate of the direct spread is at 128. According to the above, the chip rate is relatively low speed (because of the narrow-band CDMA), wherein as compared with instantaneous variations of the propagation delay, the chip period is relatively long. For this reason, an amount of deterioration in receiving characteristics is small even if characteristics of the receiving timing detecting circuit is somewhat loose. However, to perform high-speed data communications with respect to voices and other information, it is necessary to increase the bit rate and chip rate by a certain factor of multiplication which ranges between 5 and 10; in other words, it is necessary to provide the wide band CDMA. In that case, there occur other problems which the IS-95-A cannot expect. In case of the chip rate of 10 Mcps, for example, if the propagation path differs by 30

m, the receiving timing deviates from the original timing with respect to one chip only. So, it is not possible to receive signals with the original timing. In addition, a plurality of multipaths overlap with each other within a range of delay times corresponding to multiple chips. In that case, there is a problem that positions of peaks cannot be clearly defined.

A conventional example of the receiving timing detection method (or chip synchronization method) is taught by the paper entitled "Principle of Spread Spectrum Communication" which is written by Dr. Andrew J. Viterbi. The operation to capture the timing of signals which are spread by spread codes corresponding to pseudo-random codes is performed in two stages of processing. That is, the method performs initial synchronous capture (or initial synchronous search) and synchronous tracking.

The method of the initial synchronous search is explained in the fourth paragraph of Chapter 3 of the above paper. According to this method, until the correlation electric power exceeds a certain threshold value, the search is performed in a serial manner with shifting the receiving timing by a half chip space.

The synchronous tracking corresponds to the method of so-called "early-late gate" or "delay lock loop (DLL)". This method calculates first correlation electric power corresponding to the early timing which is earlier than the reference timing by the delay time Δt for the receiving and second correlation electric power corresponding to the late timing which is later by Δt . Then, the method performs fine timing adjustment in such a way that a difference between the first electric power and second electric power becomes zero.

Meanwhile, the paper of Japanese Patent Laid-Open Publication No. 4-347944 discloses some improvements to the method of the initial synchronous search and synchronous tracking. Particularly, the paper discloses the method regarding the commonality of circuits as well as the method to add tracking function to the multipath propagation path. However, the basic operation of the above method is identical to that of the aforementioned paper written by Dr. Andrew J. Viterbi. In addition, this method is not capable of solving the aforementioned problems in the wide band CDMA.

The paper of Japanese Patent Publication No. 2-39139 provides description regarding the method to search a new path wherein operation of the sliding correlator is not made only in the initial synchronous search but is made normally. Similar description is found in the paper of Japanese Patent Laid-Open Publication No. 6-284111. According to the above method which is designed to perform searching of new paths normally, it is possible to shorten the instantaneous break time in communications. However, it cannot be said that the method is capable of detecting peak positions accurately with a short time.

In short, the mobile communications system using the CDMA method performs receiving of so-called mul-

tipath signals, wherein the system should perform matching of timing with respect to each of signals. Herein, the multipath signals are transmitted to the system via multiple propagation paths which differ from each other in propagation time due to the reflection by buildings and mountains, for example. To achieve effective usage of frequencies in communications, each channel should have a capability of receiving signals under the very low E_b/N_0 environment.

Particularly, in case of the wide band CDMA method whose chip rate is 10 Mcps or so, the receiving timing is shifted by one chip when the propagation distance changes by 30 m. Such a shift makes the receiving operation impossible. A difference of propagation delay corresponding to a difference of propagation distance of 30 m or so easily occurs when a small variation occurs in the propagation path even if the distance between the base station and mobile station is unchanged. In other words, there occurs a phenomenon frequently that the receiving is performed with respect to the multipaths which overlap with each other in a range of multiple chips, and variations simultaneously occur with respect to receiving paths (i.e., emergence and vanishing of new paths).

Conventionally, the DLL technology is used for the synchronous tracking of the receiving timing. This technology is effective under prescribed conditions that each multipath has a separate peak and the propagation delay time continuously and gradually changes. In contrast, the wide band CDMA works under the condition where the receiving is performed with respect to the multipaths in an overlap manner and the delay time discontinuously changes. So, the wide band CDMA suffers from a problem due to impossibility in performance of the tracking.

SUMMARY OF THE INVENTION

It is an object of the invention to provide a CDMA chip synchronization circuit for the mobile communications system employing the wide band CDMA method so that adjustment of multiple receiving timing, particularly synchronous tracking, can be performed under a low E_b/N_0 environment.

As a result of this invention, it is possible to improve receiving quality of a wide band CDMA receiver; and it is possible to perform high-speed data transmission.

A CDMA chip synchronization circuit of this invention is provided for a mobile communications system employing a wide band CDMA method, especially direct spread code division multiple access (DS-SS) method.

In the CDMA chip synchronization circuit, a radio receiver converts radio frequency signals to digital base band signals, whilst a search section detects receiving timing with respect to multipath components contained in the digital base band signals. The detected receiving timing is used as a center position for receiving on a

time axis. The radio receiver is connected with multipath receivers, each of which contains a number of correlators which produce correlation values between the multipath components and dc-spreading codes which are delayed by different delay times respectively. Herein, the correlators correspond to prescribed intervals of time which deviate from the center position for the receiving on the time axis. Correlator outputs are temporarily stored in a memory. Then, the multipath receiver selects a correlator output having a best receiving quality from among the correlator outputs by every prescribed interval of time corresponding to a pilot period, so synchronous detection is performed using the selected correlator output. Outputs of the multipath receivers are combined at a maximum ratio, so that receiving data are produced.

Thus, the CDMA chip synchronization circuit of this invention has a capability to certainly perform detection of multipath receiving timing, particularly synchronous tracking, under a low Eb/No environment where multipaths are received in an overlap manner.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects of the subject invention will become more fully apparent as the following description is read in light of the attached drawings wherein:

FIG. 1 is a block diagram showing a CDMA chip synchronization circuit in accordance with an embodiment of the invention;

FIGs. 2A and 2B are graphs showing relationships between delay time and receiving level with respect to models of propagation characteristics of the wide band CDMA method which the invention employs; and

FIG. 3 shows an example of a signal format.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Now, a preferred embodiment of the invention will be described with reference to FIG. 1 to FIG. 3.

FIG. 1 is a block diagram showing a CDMA chip synchronization circuit in accordance with an embodiment of the invention. In FIG. 1, a radio receiver 101 receives radio frequency signals and converts them to digital base band signals. A plurality of multipath receivers, each designated by a same numeral of "112", are provided to perform decoding processes with respect to multipath components contained in the digital base band signals. Herein, each multipath receiver 112 performs a decoding process with respect to each multipath component. Then, the decoded multipath components are supplied to a RAKE combining section 107 wherein they are combined at a maximum ratio. So, the RAKE combining section 107 produces receiving data. A dc-spreading code generator 108 generates dc-spreading codes which reversely spread spectrum. A

search section 111 measures the receiving timing with respect to the multipath components.

Next, the multipath receiver 112 is configured as follows:

A delay section 109 delays the dc-spreading codes to coincide with the receiving timing which the search section 111 detects. A shift register 110 further delays the delayed dc-spreading codes, output from the delay section 109, by different delay times. Herein, the shift register section 110 has multiple output terminals corresponding to different delay times which differ from each other by a constant delay which corresponds to 1/4 chip, for example. A plurality of correlators, each designated by a same numeral of "102", produce correlation values between the digital base band signals and outputs of the shift register 110. Thus, the correlators 102 as a whole perform operation of "dc-spreading" with respect to receiving signals. A memory 103 temporarily stores (or accumulates) outputs of the correlators 102. An optimum value detector 104 and a selector 105 cooperates together to intermittently perform reading operations on the memory 103 by certain intervals of time, thus selecting a correlator output which has a best receiving quality. Using the selected correlator output, a synchronous detector 106 performs synchronous detection.

Under a real propagation environment, a number of the multipath receivers 112 is determined based on a trade-off relationship established between a maximum number in effective numbers of the multipaths and the hardware scale. Normally, in case of the city environment, it is sufficient to provide four multipath receivers per one radio signal receiver (which corresponds to one antenna). One multipath receiver 112 contains five correlators 102 which produce correlation values with respect to five timings. Herein, the timing designated by the search section 111 is used as the center of the five timings. So, there are provided five timings which are represented by 0 (i.e., center), $\pm 1/4$ chip and $\pm 1/2$ chip respectively.

In the above case, the memory 103 should have a capability to store five correlator outputs. Namely, the memory 103 stores one slot, which is partitioned by a pilot symbol, with respect to each correlator output.

The mobile station performs transmission of reverse signals which are placed in frame synchronization with forward signals which are transmitted from the base station to the mobile station. So, the search section 111 of the base station has a capability to perform path search within a prescribed range of propagation delays in accordance with a radius of a service area which covers one base station. The method of the path search for the base station is disclosed by the paper of Japanese Patent Application No. Hei 8-185103, for example.

Next, processing of the optimum value detector 104 will be explained in conjunction with FIGs. 2A and 2B.

FIGs. 2A and 2B are graphs showing relationships between delay time and receiving level with respect to

models of propagation characteristics (i.e., delay profiles) of the wide band CDMA method which the invention employs.

The above graphs are made in connection with two independent groups of multipaths, each group of which contains three paths which overlap with each other and which deviate from each other by 1/2 chip.

In case of the graph of FIG. 2A, a first group of three paths are all received with a same phase. Thus, the three paths are enhanced in receiving level so that a peak emerges at the center of the three paths on a time axis. As for a second group of three paths, a center path is received with a phase which is inverse to phases of other paths. Therefore, the three paths are canceled with each other in receiving level, so that receiving level of the center path should become very small. For this reason, two sub-peaks emerge in the receiving level regarding the second group of paths.

In case of the graph of FIG. 2B, as for a first group of three paths, only a last path is received with an inverse phase, so that a position of a peak is shifted in a backward direction from a center position by 1/2 chip on a time axis. In addition, a small sub-peak emerges at a position which is 1/2 chip after the center position. As for a second group of three paths, two paths other than a first path are received with inverse phases, so a position of a peak delays from a center position by 1/2 chip.

As described above, in the case where the system (e.g., station) receives multiple multipaths in an overlap manner with small shifts of phases, even if the paths do not change in receiving timing and receiving level, a peak in an overall receiving level fluctuates in position and level.

The receiver applicable to this invention is designed as follows:

A search section detects positions with respect to groups of paths, to which multipath receivers are assigned respectively. Herein, each multipath receiver uses the timing that the search section detects as a center position for receiving on a time axis. So, the multipath receiver has multiple correlators which perform dc-spreading on receiving signals with respect to both of forward and backward directions from the center position on the time axis. That is, the correlators are provided to cope with delays of the timing which correspond to $\pm 1/2$ chip and $\pm 1/4$ chip from the center position. Then, the multipath receiver selects a correlator output having a best receiving quality from among correlator outputs which are provided with certain intervals of time. So, the multipath receiver performs decoding of the selected correlator output.

In case of the second group of paths shown in FIG. 2A, the sub-peaks emerge at different timings which separate from each other by 1 chip or more, it can be presumed that noise contained in one sub-peak is independent from noise contained in another sub-peak. In case of the first group of paths shown in FIG. 2B, a relatively large sub-peak emerges at the timing apart from

the peak by 1 chip or more.

The present embodiment can be modified to cope with the above cases. That is, the present embodiment can be modified in such a way that two correlator outputs corresponding to two peaks (or sub-peaks) are extracted and combined.

FIG. 3 shows an example of a signal format applicable to this invention. Herein, 'PL' designates a pilot symbol.

As shown in FIG. 3, a "known" pilot signal is periodically inserted into transmission of data by a constant period (i.e., pilot period which is set at 0.625 ms, for example) which is shorter than a fading period. In that case, the above pilot signal can be used as a reference signal for synchronous detection, details of which will be described below.

The pilot period is used as a partition of transmission. So, multiple correlator outputs are stored in the memory. The system measures receiving quality of signals contained in the pilot period with respect to each of the correlators. Then, the system selects a correlator output having a highest receiving quality. Or, if a sub-peak is detected at a position which sufficiently separates from the timing (i.e., peak position) of the correlator having the highest receiving quality and which is considered to be independent from noise, the system extracts a correlator output corresponding to the sub-peak from the memory. Thus, the synchronous detection is performed by using the pilot signal as the reference signal representing carrier phase.

Incidentally, it is possible to employ a variety of methods for determination of the receiving quality for each of the correlator outputs, as follows:

- (1) Determination is made based on the receiving level of the pilot signal.
- (2) If the pilot signal is constructed by multiple symbols, determination is made based on a ratio between a square of an average value (i.e., presumed value of signal power) and a variance (i.e., presumed value of noise power).
- (3) Determination is made by measuring receiving levels with respect to the pilot signal portion as well as the data portion.
- (4) Temporary decision is made with respect to the data portion. Reverse modulation is effected on the receiving data on the basis of the result of the temporary decision, so phases of all data are made uniform with the carrier phase. Then, determination is made based on a ratio between a square of an average value (i.e., presumed value of signal power) and a variance (i.e., presumed value of noise power).

Finally, this invention is capable of demonstrating a variety of effects, which the conventional technology cannot provide, as follows:

(1) It is possible to perform fine adjustment for the optimum receiving timing by a certain period, e.g., a pilot period for insertion of a pilot signal into transmission of data. So, even in the wide band CDMA under a propagation environment where the receiver performs receiving with respect to multipaths which overlap with each other, it is possible to perform synchronous tracking to follow variations of peaks in receiving level. Namely, it is possible to perform receiving in a stable manner.

(2) It is possible to loosen a detection precision of the search section. For this reason, it is possible to reduce a time for averaging at a search mode. Therefore, it is possible to perform fast detection of a new path even if a propagation path rapidly changes.

As this invention may be embodied in several forms without departing from the spirit of essential characteristics thereof, the present embodiment is therefore illustrative and not restrictive, since the scope of the invention is defined by the appended claims rather than by the description preceding them, and all changes that fall within metes and bounds of the claims, or equivalence of such metes and bounds are therefore intended to be embraced by the claims.

Claims

1. A CDMA chip synchronization circuit, which is provided for a receiver of a mobile communications system employing a direct spread code division multiple access (DS-CDMA) method, comprising:
 - search means (111) for detecting receiving timing with respect to a plurality of multipath components contained in receiving signals;
 - a plurality of receiving means (102), each of which is provided for each of the receiving signals, wherein the receiving timing detected by the search means is set as a center position for receiving on a time axis while a plurality of positions are set for the receiving to deviate from the center position on the time axis by prescribed intervals of time which are shorter than a 1-chip period;
 - a memory (103) for temporarily storing outputs of the plurality of receiving means; and
 - selecting means (104, 105) for selecting a receiving signal having a best receiving quality from among the receiving signals received by the plurality of receiving means respectively by every constant interval of time.
2. A CDMA chip synchronization circuit as defined in claim 1 wherein the selecting means changes over the receiving signal selected thereby by an interval of time which is shorter than a fading period of a

propagation path and in which averaging process can be performed with respect to receiving qualities of the receiving signals.

3. A CDMA chip synchronization circuit as defined in claim 1 wherein if an interval of time between a first receiving timing of a first receiving signal having a first best receiving quality and a second receiving timing of a second receiving signal having a second best receiving quality is shorter than a prescribed interval of time, the selecting means selects both of the first and second receiving signals.
4. A CDMA chip synchronization circuit as defined in claim 1 wherein decision for a receiving quality is made based on an amount of electric power of a receiving signal.
5. A CDMA chip synchronization circuit as defined in claim 1 wherein decision for a receiving quality is made based on a ratio between electric power of a receiving signal and interference electric power.
6. A CDMA chip synchronization circuit, which is provided for a mobile communications system employing a direct spread code division multiple access (DS-CDMA) method, comprising:

a radio receiver (101) for converting radio frequency signals to digital base band signals;
 a plurality of multipath receivers (112) for performing decoding processes respectively on multipath components contained in the digital base band signals;
 a RAKE combining section (107) for combining the multipath components, decoded by the multipath receivers, at a maximum ratio, thus producing receiving data;
 a dc-spreading code generator (108) for generating dc-spreading codes for performing dc-spreading of spectrum with respect to the digital base band signals; and
 search means (111) for detecting receiving timing with respect to the multipath components contained in the digital base band signals,
 wherein each of the multipath receivers comprises

delay means (109) for delaying the dc-spreading codes to coincide with the receiving timing detected by the search means;
 a shift register (110) having a plurality of output terminals corresponding to delay times, an interval of which is constant and is shorter than a 1-chip period, by which the delayed dc-spreading codes delayed by the delay means are further delayed

respectively;

a plurality of correlators (102) for performing the dc-spreading of the digital base band signals by producing correlation values between the digital base band signals and outputs of the shift register respectively;

a memory (103) for temporarily storing outputs of the plurality of correlators;

selecting means (104, 105) for performing reading operation of the memory by every constant interval of time so as to select a correlator output having a best receiving quality from among correlator outputs provided by the correlators respectively; and
synchronous detection means (106) for performing synchronous detection using the correlator output selected by the selecting means.

for the selecting means corresponds to a pilot period for inserting a pilot signal into transmission of data, and wherein the pilot period is shorter than a fading period of a propagation path.

7. A CDMA chip synchronization circuit, which is provided for a mobile communications system employing a direct spread code division multiple access (DS-CDMA) method, comprising:

a radio receiver (101) for converting radio frequency signals to digital base band signals;
search means (111) for detecting receiving timing with respect to multipath components contained in the digital base band signals, wherein the detected receiving timing is used as a center position for receiving on a time axis;

a plurality of multipath receivers (112), each of which contains a plurality of correlators (102) for producing correlation values between the multipath components and dc-spreading codes which are respectively delayed by intervals of time which are shorter than a 1-chip period, wherein the correlators correspond to different intervals of time which deviate from the center position for the receiving on the time axis;

a memory (103) for temporarily storing correlator outputs provided from the correlators respectively;

selecting means (104, 105) for selecting a correlator output having a best receiving quality from among the correlator outputs by every prescribed interval of time;

synchronous detection means for performing synchronous detection using the selected correlator output, thus providing an output of the multipath receiver; and

combining means (107) for combining outputs of the multipath receivers at a maximum ratio, thus producing receiving data.

8. A CDMA chip synchronization circuit as defined in claim 7 wherein the prescribed interval of time set

FIG.1

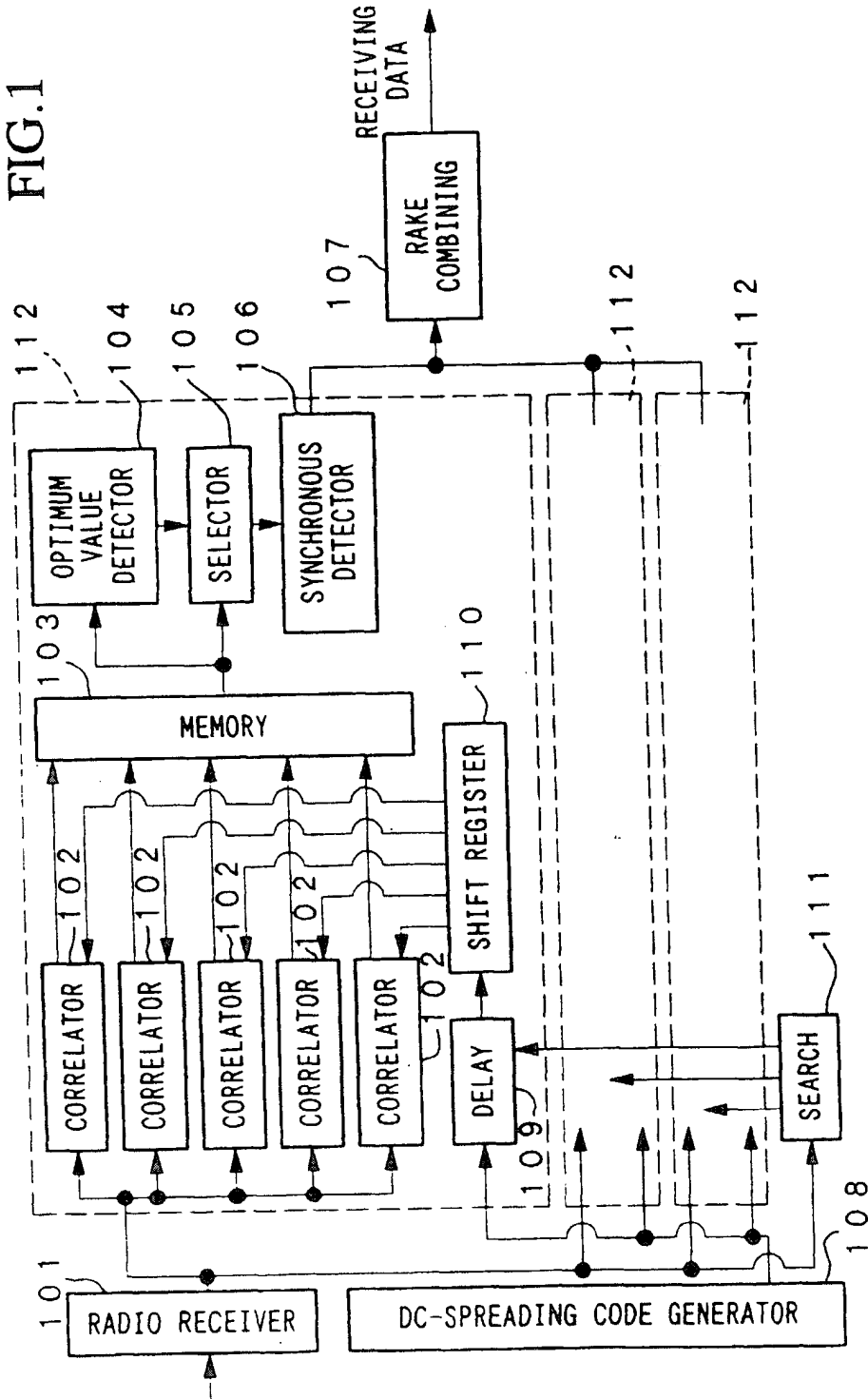


FIG.2A

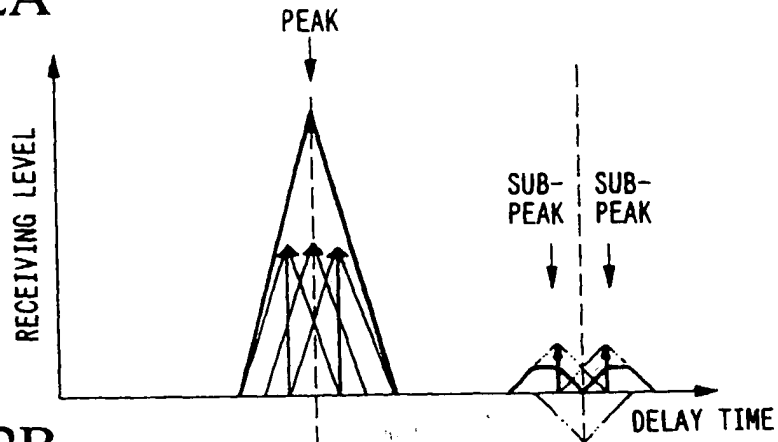


FIG.2B

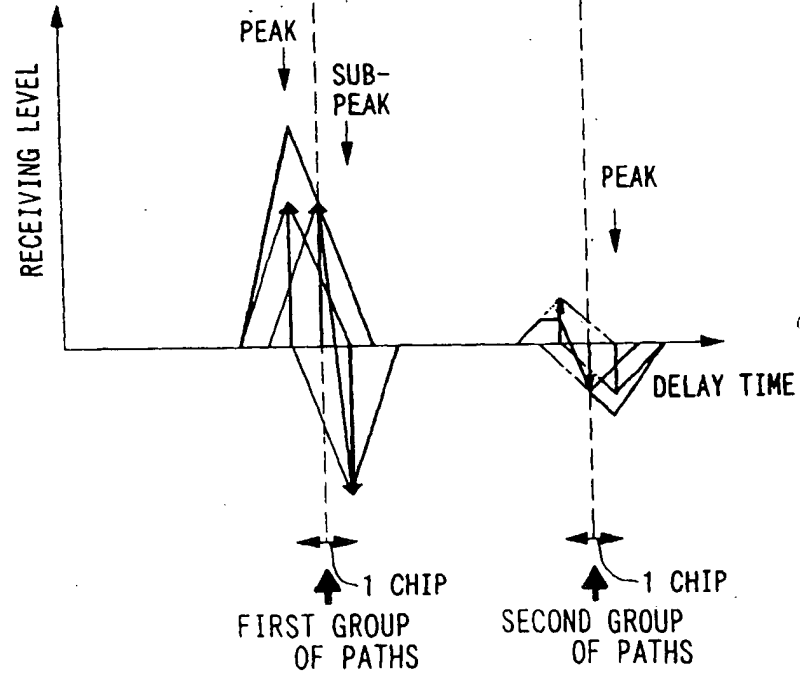


FIG.3



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(54) CDMA chip synchronization circuit

(57) A CDMA chip synchronization circuit is provided for a mobile communications system employing a wide band CDMA method, especially direct spread code division multiple access (DS-CDMA) method, and is designed to have a capability to certainly perform detection of multipath receiving timing, particularly synchronous tracking, under a low E_b/N_0 environment where multipaths are received in an overlap manner. Herein, a radio receiver (101) converts radio frequency signals to digital base band signals, whilst a search section (111) detects receiving timing with respect to multipath components contained in the digital base band signals. The detected receiving timing is used as a center position for receiving on a time axis. The radio receiver is connected with mul-

tipath receivers (112), each of which contains a number of correlators (102) which produce correlation values between the multipath components and dc-spreading codes which are delayed by different delay times respectively. Herein, the correlators correspond to prescribed intervals of time which deviate from the center position for receiving on the time axis. Correlator outputs are temporarily stored in a memory (103). Then, the multipath receiver selects a correlator output having a best receiving quality from among the correlator outputs by every prescribed interval of time corresponding to a pilot period, so synchronous detection is performed using the selected correlator output. Outputs of the multipath receivers are combined at a maximum ratio, so that receiving data are produced.

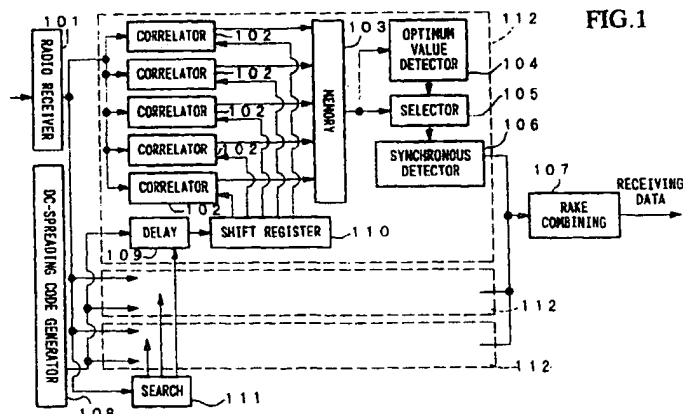


FIG. 1

EP 0 848 503 A3



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Application Number
EP 97 12 1342

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